CLAIMS

What is claimed is:

1. A method for fabricating a plasma probe, comprising:

providing a substantially planar sacrificial substrate;

forming a plurality of first conductive structures on said sacrificial substrate;

providing a semiconductor substrate;

forming a dielectric layer on said semiconductor substrate;

forming a plurality of second conductive structures on said dielectric layer, each second conductive structure of said plurality of second conductive structures corresponding to a first conductive structure of said first plurality of conductive structures;

securing a dielectric film over said plurality of second conductive structures;

orienting said plurality of first conductive structures over corresponding ones of said plurality of second conductive structures, said plurality of first conductive structures and said plurality of second conductive structures both being secured to said dielectric film;

removing said sacrificial substrate; and

removing material of said dielectric film exposed between adjacent first conductive structures of said plurality of first conductive structures.

2. The method of claim 1, wherein said forming said plurality of second conductive structures comprises forming said plurality of second conductive structures such that distances therebetween approximate distances between features on a fabrication substrate to undergo substantially the same processing as that to be monitored with the plasma probe.

3. The method of claim 1, wherein said forming said plurality of second conductive structures comprises forming a plurality of sets of conductive structures, each of said plurality of sets being located at a different elevation than every other set of said plurality of sets to facilitate generation of a three-dimensional representation of at least one characteristic of a plasma to be monitored.

4. The method of claim 3, wherein said forming said plurality of sets comprises forming conductive structures in each set of said plurality that correspond to and are in substantial alignment with conductive structures in every other set of said plurality.

5. The method of claim 4, wherein said forming said plurality of sets comprises forming every conductive structure of each set to be in substantially alignment with a corresponding conductive structure of every other set.

6. The method of claim 3, wherein said forming said plurality of sets comprises forming each of said plurality of sets at elevations, relative to a plane of said first plurality of conductive structures, which correspond substantially to heights of features on a fabrication substrate to undergo substantially the same processing as that to be monitored with the plasma probe.

7. The method of claim 1, further comprising electrically connecting selected first conductive structures of said plurality of first conductive structures to meters.

8. The method of claim 7, further comprising electrically connecting at least one second conductive structure of said plurality of second conductive structures to a second meter.

9. The method of claim 1, wherein said providing said sacrificial substrate comprises providing a sacrificial substrate comprising at least one of nylon and polystyrene.

10. The method of claim 1, wherein said removing said sacrificial substrate comprises exposing said sacrificial substrate to a degradative temperature.

11. The method of claim 1, wherein said removing said sacrificial substrate comprises exposing said sacrificial substrate to a solvent for a material thereof.

12. The method of claim 1, wherein said forming said plurality of first conductive structures comprises forming a conductive layer on a surface of said sacrificial substrate and patterning said conductive layer.

13. The method of claim 1, wherein said providing said semiconductor substrate comprises providing a semiconductor substrate of a same type as a semiconductor substrate upon which a material layer is to be formed using a plasma.

14. The method of claim 1, wherein said providing said semiconductor substrate comprises providing a silicon-on-insulator type substrate.

15. The method of claim 14, wherein said providing said silicon-on-insulator type substrate comprises providing at least one of a silicon-on-glass substrate, a silicon-on-sapphire substrate, and a silicon-on-ceramic substrate.

16. The method of claim 1, wherein said providing said semiconductor substrate comprises providing at least a partial wafer of semiconductive material.

17. The method of claim 16, wherein said providing said at least said partial wafer of semiconductive material comprises providing at least a partial wafer comprising at least one of silicon, gallium arsenide, and indium phosphide.

18. The method of claim 1, wherein said forming said dielectric layer comprises growing an oxide on a surface of said semiconductor substrate.

19. The method of claim 1, wherein said forming said dielectric layer comprises depositing dielectric material onto a surface of said semiconductor substrate.

20. The method of claim 1, wherein said forming said plurality of second conductive structures comprises:

forming a layer comprising conductive material on said dielectric layer; and

patterning said layer comprising conductive material.

21. The method of claim 1, wherein said securing said dielectric film comprises securing a dielectric film comprising polyimide.

22. The method of claim 1, wherein said removing material of said dielectric film comprises exposing said dielectric film to at least one of a solvent and an etchant for a material thereof.

23. A plasma probe, comprising:

a semiconductor substrate;

a first dielectric layer formed on said semiconductor substrate;

at least one first electrode formed on said first dielectric layer;

a dielectric structure formed on at least portions of said at least one first electrode, dimensions of said portions of said at least one first electrode along a plane of said at least one first electrode being substantially the same as corresponding dimensions of said dielectric structure along a plane of said dielectric structure that is parallel to said plane of said at least one first electrode; and

at least one second electrode on said dielectric structure, dimensions of said at least one second electrode along a plane thereof being substantially the same as said corresponding dimensions of said dielectric structure.

24. The plasma probe of claim 23, wherein a distance between said plane of said at least one first electrode and said plane of said at least one second electrode is substantially the same as a height of at least one feature on a fabrication substrate to undergo substantially the same processing as that to be monitored by the plasma probe.

25. The plasma probe of claim 23, wherein said at least one second electrode comprises a plurality of second electrode sets, each being located in a different plane oriented substantially parallel to said plane of said at least one first electrode, so as to facilitate generation of a three-dimensional representation of at least one characteristic of a plasma to be monitored with the plasma probe.

26. The plasma probe of claim 25, wherein a plane of each second electrode set is located at an elevation relative to said plane of said at least one first electrode which corresponds to an elevation of a feature on a fabrication substrate to undergo substantially the same processing as that to be monitored by the plasma probe.

27. The plasma probe of claim 23, comprising a plurality of second electrodes.

28. The plasma probe of claim 27, wherein adjacent second electrodes of said plurality of second electrodes are spaced apart from one another a distance which is substantially the same as a corresponding lateral distance of a feature of a fabrication substrate to undergo substantially the same processing as that to be monitored by the plasma probe.

29. The plasma probe of claim 23, wherein said at least one first electrode is configured to communicate with a meter.

30. The plasma probe of claim 23, wherein said at least one second electrode is configured to communicate with a meter.

31. The plasma probe of claim 23, comprising a plurality of electrically distinct second electrodes.

32. The plasma probe of claim 31, wherein portions of said at least one first electrode are exposed between adjacent second electrodes of said plurality of second electrodes.

33. The plasma probe of claim 31, further comprising at least one other first electrode, said at least one other first electrode being in a different plane than both said at least one first electrode and said plurality of second electrodes.

34. The plasma probe of claim 23, wherein said semiconductor substrate comprises a same type of semiconductor substrate as that with which the plasma probe is to be used.

35. The plasma probe of claim 23, wherein said semiconductor substrate comprises a silicon-on-insulator type substrate.

36. The plasma probe of claim 35, wherein said silicon-on-insulator type substrate comprises one of a silicon-on-glass substrate, a silicon-on-sapphire substrate, and a silicon-on-ceramic substrate.

37. The plasma probe of claim 23, wherein said semiconductor substrate comprises at least a partial wafer comprising semiconductive material.

38. The plasma probe of claim 37, wherein said semiconductive material comprises at least one of silicon, gallium arsenide, and indium phosphide.

39. The plasma probe of claim 23, wherein said dielectric structure comprises polyimide.

40. A method for evaluating characteristics of a plasma, comprising:

introducing at least one first semiconductor substrate upon which at least one semiconductor device is being fabricated into a reaction chamber;

introducing a probe into said reaction chamber under substantially the same conditions as those present when said at least one semiconductor substrate is located within said reaction chamber, said probe including a second semiconductor substrate of a same type as said at least one first semiconductor substrate and having substantially the same dimensions as said at least one first semiconductor substrate; and

evaluating at least one characteristic of the plasma with said probe across a plurality of locations of said probe while the plasma is being generated.

41. The method of claim 40, wherein said introducing said probe comprises introducing a plurality of probes into said reaction chamber.

42. The method of claim 40, wherein said introducing said probe comprises introducing said probe into said reaction chamber in substantially a same orientation as an orientation of said at least one first semiconductor substrate within said reaction chamber.

43. The method of claim 42, wherein said introducing said probe comprises introducing said probe into said reaction chamber in a substantially vertical orientation.

44. The method of claim 42, wherein said introducing said probe comprises introducing said probe into said reaction chamber in a substantially horizontal orientation.

45. The method of claim 40, wherein said introducing said at least one first semiconductor substrate comprises introducing a plurality of first semiconductor substrates into said reaction chamber.

46. The method of claim 40, wherein said introducing said at least one first semiconductor substrate comprises introducing said at least one first semiconductor substrate into said reaction chamber in a substantially vertical orientation.

47. The method of claim 40, wherein said introducing said at least one first semiconductor substrate comprises introducing said at least one first semiconductor substrate into said reaction chamber in a substantially horizontal orientation.

48. The method of claim 40, wherein said introducing said probe comprises introducing said probe into said reaction chamber while said at least one first semiconductor substrate is located within said reaction chamber.

49. The method of claim 40, wherein said introducing said probe comprises introducing said probe into said reaction chamber in a same location as said at least one semiconductor substrate following exposure of said at least one semiconductor substrate to the plasma.

50. The method of claim 40, wherein said introducing said probe comprises introducing said probe into said reaction chamber in a same location as said at least one semiconductor substrate prior to exposure of said at least one semiconductor substrate to the plasma.

51. The method of claim 40, wherein said evaluating comprises communicating a plurality of electrical signals from a corresponding plurality of locations across a surface of said probe to a corresponding plurality of meters.

52. The method of claim 40, wherein said evaluating is effected during exposure of said probe to the plasma.

53. The method of claim 40, wherein said evaluating is effected following exposure of said probe to the plasma.

54. The method of claim 53, wherein said evaluating comprises evaluating a charge stored by capacitors of said probe while said probe was exposed to the plasma.

55. The method of claim 40, further comprising, based on said evaluating, generating a three-dimensional representation of a state of said at least one first semiconductor substrate during exposure thereof to said plasma.

56. The method of claim 40, wherein said evaluating comprises evaluating said at least one characteristic at a plurality of elevations of each location of said plurality of locations of said probe.

57. The method of claim 40, wherein said evaluating comprises evaluating said at least one characteristic at at least one elevation at at least one location on said probe that corresponds to at least one elevation of a feature at a corresponding location of a fabrication substrate to be subjected to substantially the same processing as said probe.

58. The method of claim 40, wherein said evaluating comprises evaluating said at least one characteristic at a plurality of locations which correspond to lateral edges of at least one feature on a fabrication substrate to be subjected to substantially the same processing as said probe.

59. The method of claim 40, wherein said evaluating comprises generating data corresponding to said at least one characteristic.

60. The method of claim 59, further comprising collecting said data.

61. A plasma probe system, comprising:

a plasma probe including:

a semiconductor substrate; and

a plurality of probe elements positioned on a surface of said semiconductor substrate, said plurality of probe elements being positioned so as to represent at least one feature on a fabrication substrate to undergo substantially the same processing as that to be monitored by said plasma probe;

a plurality of meters configured to electrically communicate with corresponding probe elements of said plurality of probe elements; and

diagnostic apparatus configured to electrically communicate with each meter of said plurality of meters to measure at least one characteristic of a plasma at locations of each probe element of said plurality of probe elements.

62. The system of claim 61, wherein at least two of said plurality of probe elements are in substantial alignment with one another at different elevations.

63. The system of claim 62, wherein said plurality of probe elements includes at least three sets of electrodes, each set of electrodes comprising a plurality of electrodes that are located in substantially the same plane, different sets of said plurality of sets being located in different planes so as to facilitate generation of a three-dimensional representation of said at least one characteristic of said plasma.

64. The system of claim 63, wherein each electrode of said plurality of electrodes of each set of said plurality of sets is in substantial alignment with at least two electrodes of two other sets of said plurality of sets.

65. The system of claim 63, wherein said different planes are located at elevations, relative to a lowermost set of said plurality of sets, which correspond to elevations of features of

a fabrication substrate to be subjected to substantially the same processing as that to be monitored by said plasma probe.

66. The system of claim 61, wherein said semiconductor substrate has dimensions that are similar to dimensions of semiconductor device substrates upon which plasma processes are to be performed and with which said plasma probe is to be used.

67. The system of claim 61, wherein said semiconductor substrate is formed from a semiconductor material of a same type as a semiconductor material of semiconductor device substrates upon which plasma processes are to be performed and with which said plasma probe is to be used.

68. The system of claim 61, wherein each of said plurality of meters is configured to sense at least one characteristic of said plasma while said plasma is being generated.

69. The system of claim 61, wherein each probe element of said plurality of probe elements includes a first electrode, a second electrode, and a dielectric layer between said first and second electrodes.

70. The system of claim 69, wherein said dielectric layer comprises polyimide.

71. The system of claim 69, wherein said plasma probe includes probe elements with dielectric layers of different thicknesses.

72. The system of claim 61, wherein said semiconductor substrate comprises a silicon-on-insulator substrate.

73. The system of claim 72, wherein said silicon-on-insulator substrate comprises one of a silicon-on-glass substrate, a silicon-on-sapphire substrate, and a silicon-on-ceramic substrate.

74. The system of claim 61, wherein said semiconductor substrate comprises at least a portion of a wafer comprising semiconductive material.

75. The system of claim 74, wherein said semiconductive material comprises one of silicon, gallium arsenide, and indium phosphide.